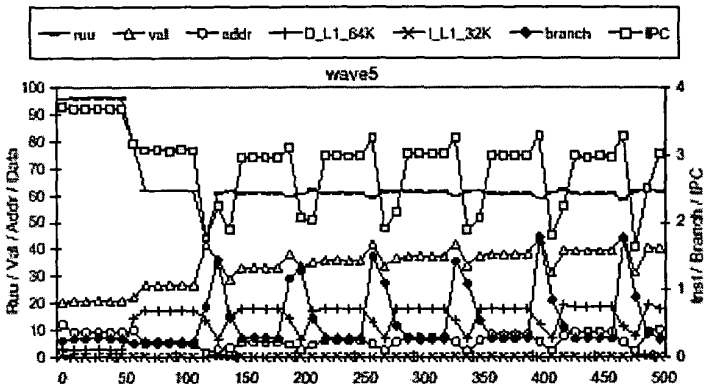

FIG. 1

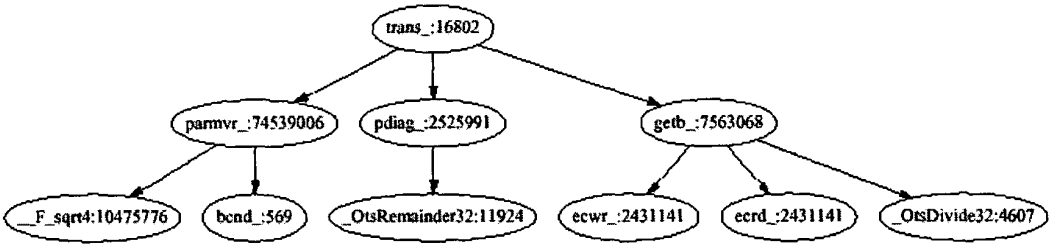

FIG. 2

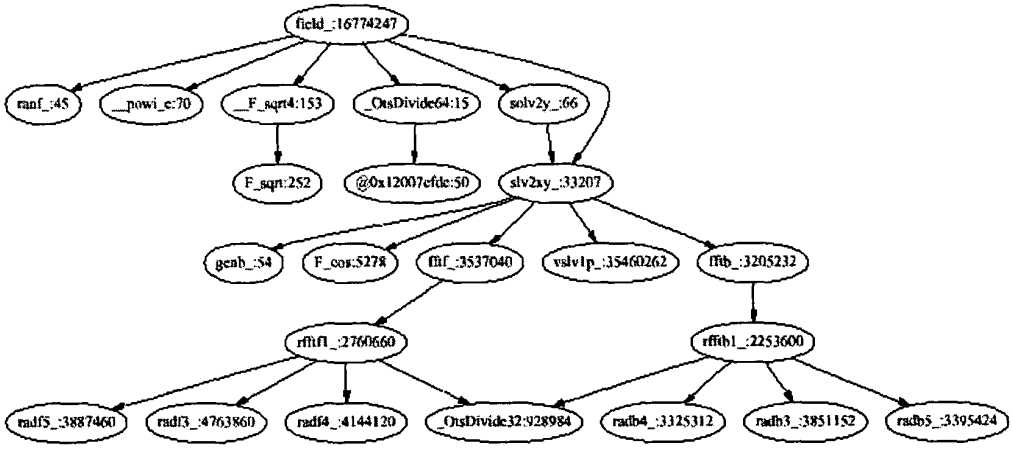

FIG. 3

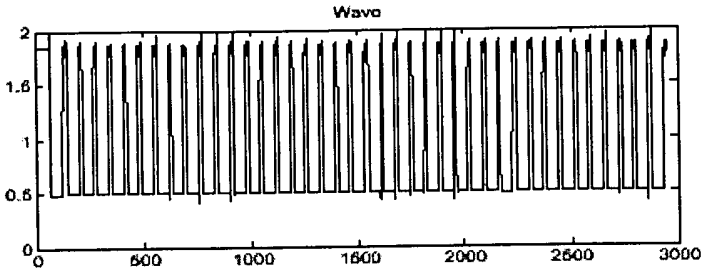

FIG. 4A

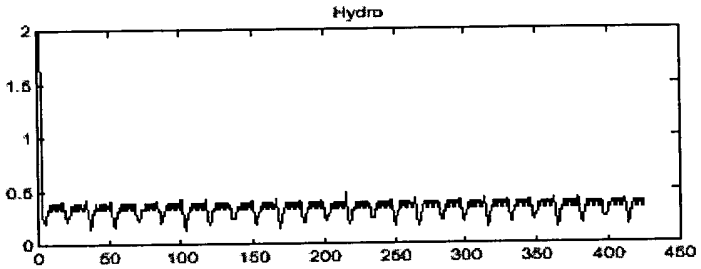

FIG. 4B

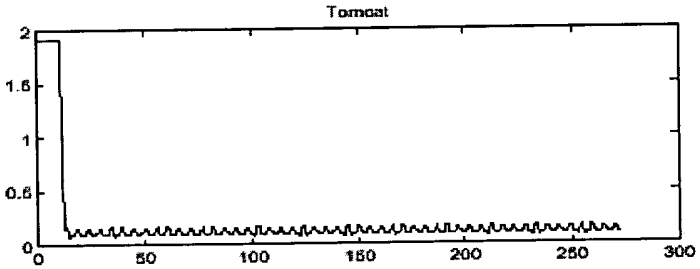

FIG. 4C

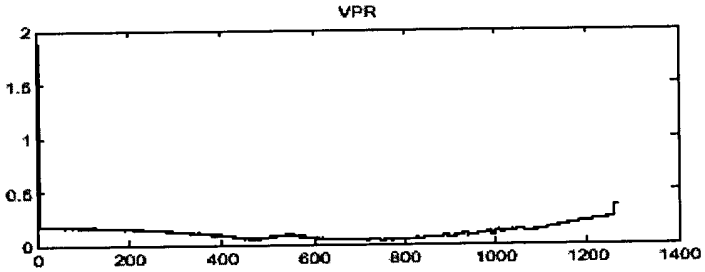

FIG. 4D

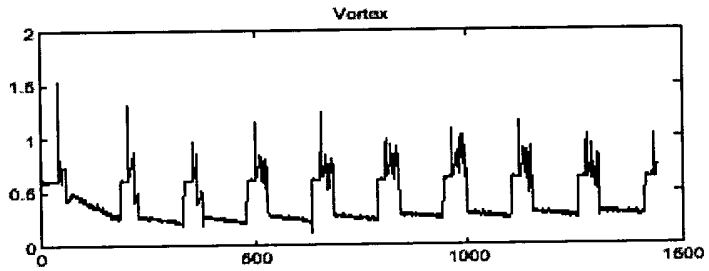

FIG. 4E

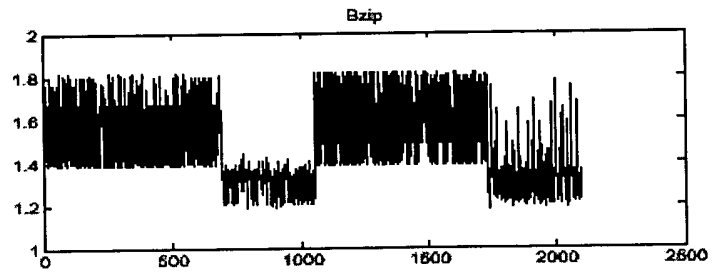

FIG. 4F

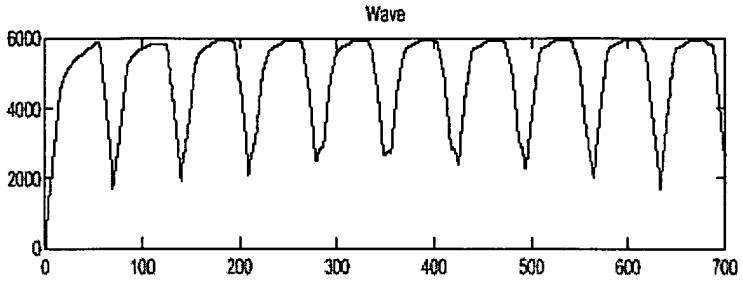

FIG. 5A

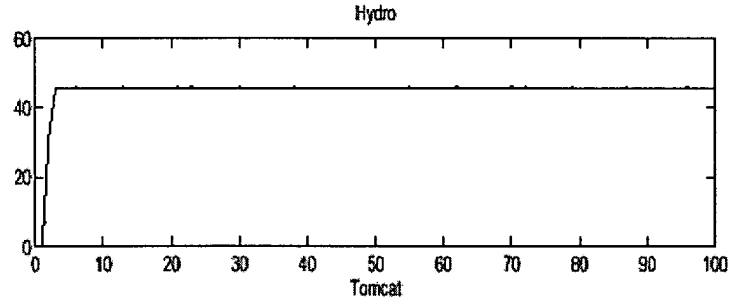

FIG. 5B

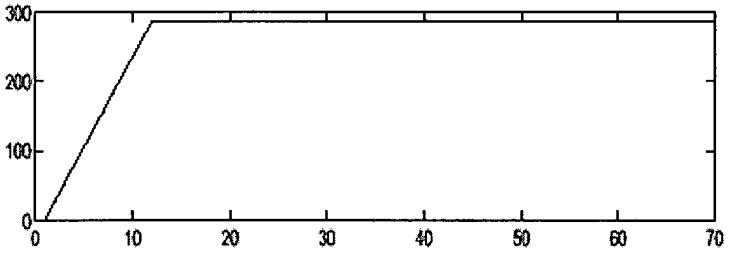

FIG. 5C

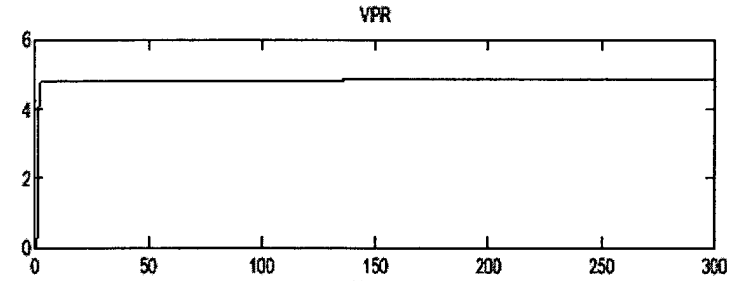

FIG. 5D

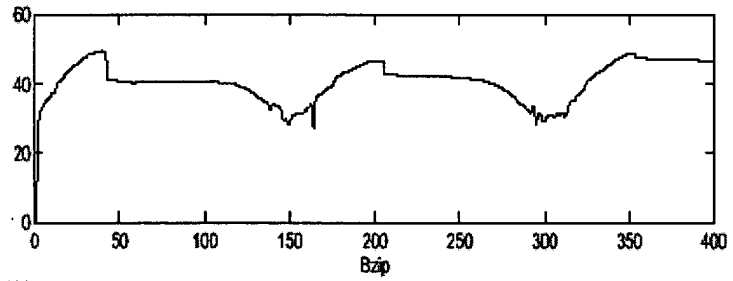

FIG. 5E

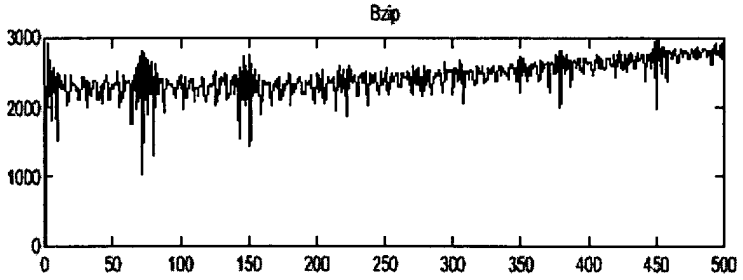

FIG. 5F

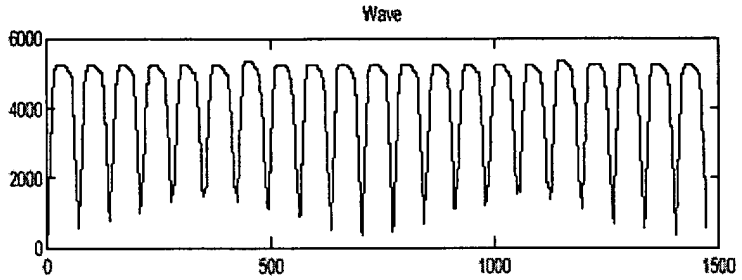

FIG. 6A

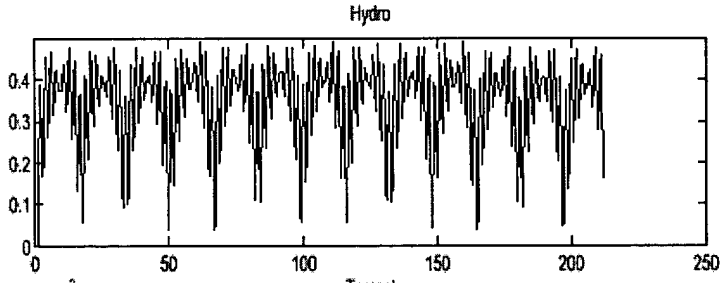

FIG. 6B

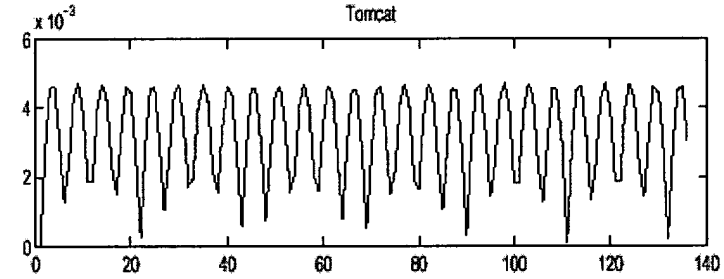

FIG. 6C

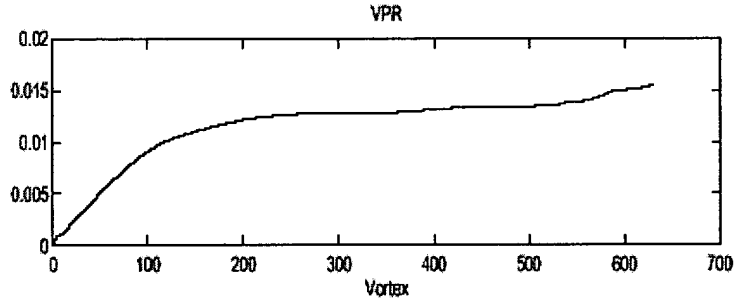

FIG. 6D

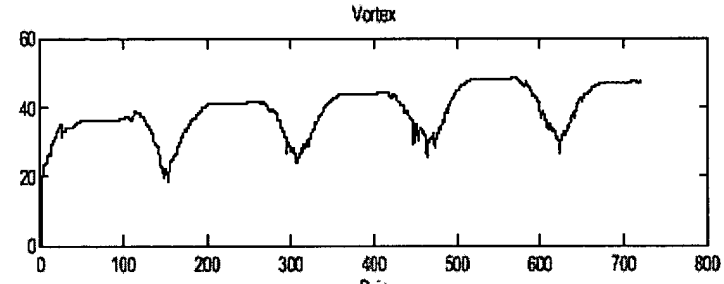

FIG. 6E

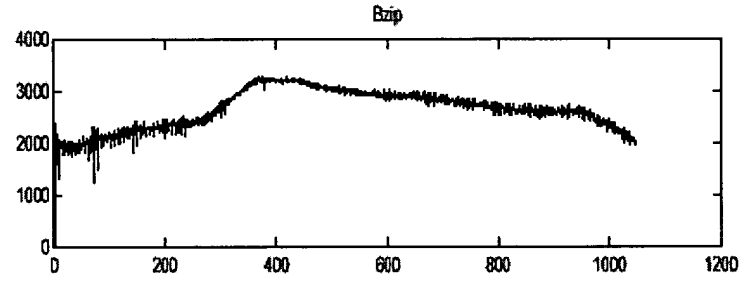

FIG. 6F

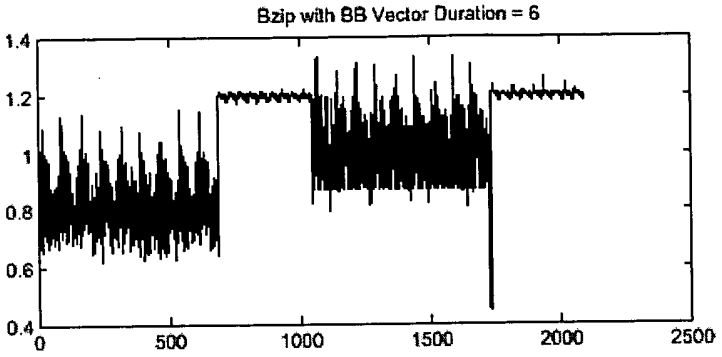

FIG. 7A

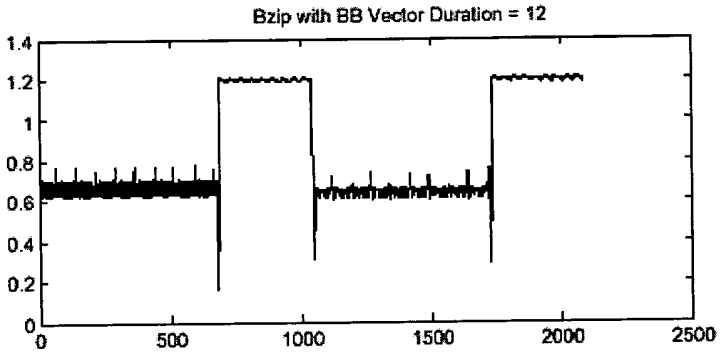

FIG. 7B

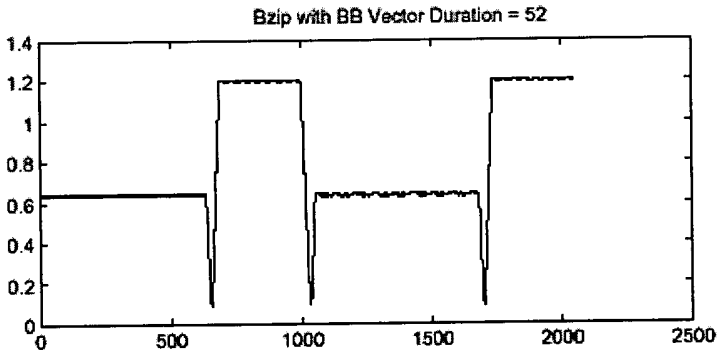

FIG. 7C

Instruction Cache	32k 2-way set-associative, 32 byte blocks, 1 cycle latency
Data Cache	64k 4-way set-associative, 32 byte blocks, 2 cycle latency
Unified L2 Cache	1Meg 4-way set-associative, 32 byte blocks, 12 cycle latency
Branch Predictor	hybrid - 8-bit gshare w/ 8k 2-bit predictors + a 8k bimodal predictor
Out-of-Order Issue	out-of-order issue of up to 8 operations per cycle, 128 entry re-order buffer
Mechanism	load/store queue, loads may execute when all prior store addresses are known
Architecture Registers	32 integer, 32 floating point
Functional Units	8-integer ALU, 4-load/store units, 2-FP adders, 2-integer MULT/DIV, 2-FP MULT/DIV
Virtual Memory	8K byte pages, 30 cycle fixed TLB miss latency after earlier-issued instructions complete

FIG. 8

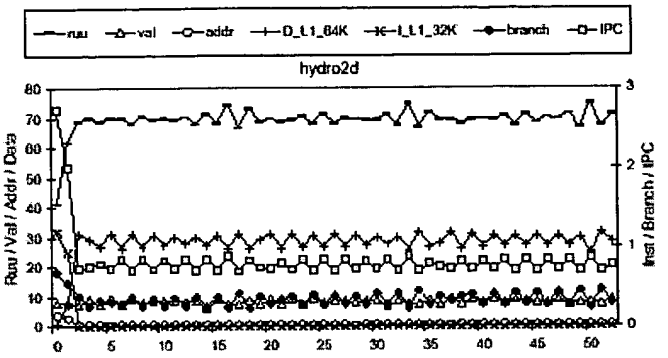

FIG. 9A

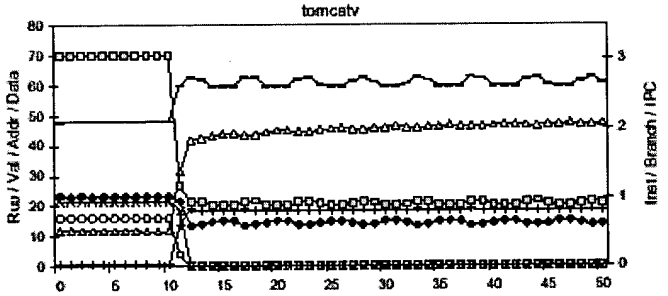

FIG. 9B

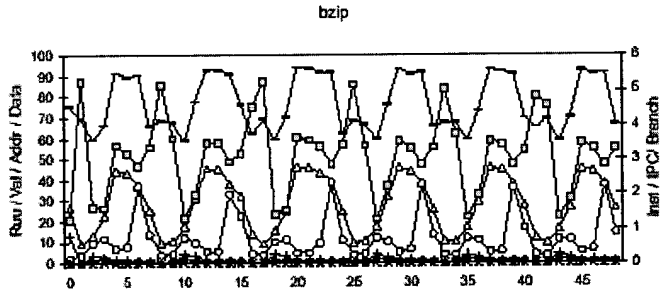

FIG. 9C

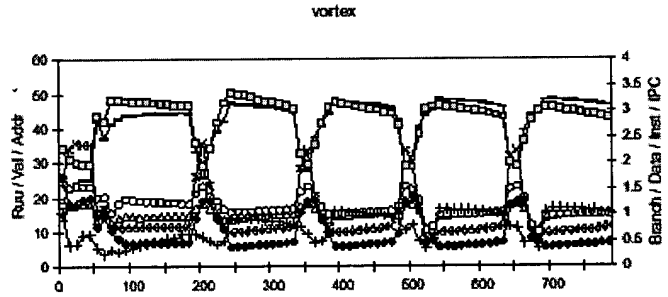

FIG. 9D

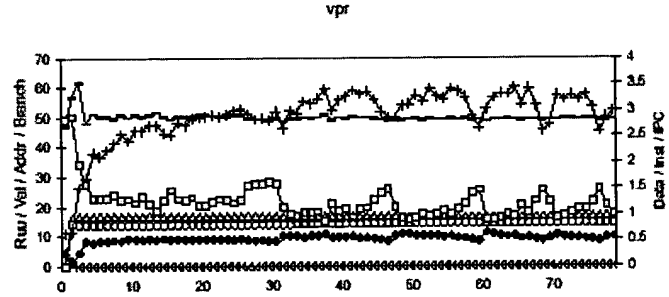

FIG. 9E

name	init	period	bpred	ruu	IPC	d miss	i miss	val miss	addr miss
bzip	2	9	4.2%	75.8%	2.681	1.7%	0.000%	25.1%	13.3%
hydro	5	17	0.4%	68.7%	0.793	14.6%	0.022%	8.3%	0.6%
tomcat	13	5	0.8%	59.6%	0.955	9.7%	0.043%	46.2%	1.0%
vortex	40	144	0.6%	43.4%	2.726	0.9%	0.979%	15.2%	16.4%
vpr	4	2	9.3%	49.8%	1.143	3.0%	0.001%	16.6%	14.2%
wave	68	70	0.6%	62.2%	2.596	7.4%	0.000%	38.1%	7.9%

FIG. 10

name	start	bpred	err	ruu	err	IPC	err	data	err	inst	err	val	err	addr	err
bzip	150	4.2%	1%	75.4%	0.5%	2.8	5.1%	1.3%	25.8%	0.0%	-	25.4%	1.1%	15.7%	17.9%
hydro	6	0.3%	16%	69.8%	1.7%	0.8	2.5%	14.8%	1.5%	0.0%	-	8.2%	1.8%	0.6%	9.1%
tomcat	12	0.8%	3%	60.5%	1.5%	0.9	1.5%	9.8%	1.1%	0.0%	-	41.1%	12.4%	0.9%	17.1%
vortex	382	0.6%	2%	43.7%	0.8%	2.8	1.9%	0.9%	1.2%	1.0%	2.8%	15.2%	0.1%	16.3%	0.7%
vpr	746	9.0%	3%	49.7%	0.3%	1.2	4.3%	3.1%	6.4%	0.0%	-	16.6%	0.0%	14.4%	1.3%
wave	127	0.6%	9%	60.7%	2.5%	2.5	3.3%	7.7%	4.4%	0.0%	-	40.4%	6.1%	8.5%	7.8%

FIG. 11

name	start	bpred	err	ruu	err	IPC	err	data	err	inst	err	val	err	addr	err
bzip	1733	4.0%	6%	63.8%	18.8%	2.5	5.9%	1.8%	8.0%	0.0%	–	14.2%	77.2%	7.3%	82.0%
hydro	36	0.3%	12%	69.2%	0.9%	0.8	3.9%	14.8%	1.4%	0.0%	–	8.4%	0.4%	0.6%	9.3%
tomcat	144	0.8%	1%	60.9%	2.2%	1.0	1.9%	9.5%	2.0%	0.1%	–	39.8%	16.2%	1.1%	13.7%
vortex	330	0.6%	3%	41.9%	3.6%	2.8	3.4%	0.7%	16.3%	1.0%	4.0%	15.7%	3.8%	17.7%	7.7%
vpr	746	9.0%	3%	49.7%	0.3%	1.2	4.3%	3.1%	6.4%	0.0%	–	16.6%	0.0%	14.4%	1.3%
wave	1036	0.3%	84%	61.5%	1.2%	2.8	6.0%	7.9%	6.7%	0.0%	–	37.0%	2.8%	6.5%	20.8%

FIG. 12

name	start	bpred	err	ruu	err	IPC	err	data	err	inst	err	val	err	addr	err
bzip	11	4.9%	17%	74.3%	2.0%	2.2	23.2%	2.8%	68.9%	0.0%	–	22.7%	10.8%	8.5%	55.4%
hydro	22	0.3%	12%	69.6%	1.4%	0.8	2.4%	14.8%	1.7%	0.0%	–	8.5%	1.8%	0.6%	8.6%
tomcat	18	0.6%	28%	61.0%	2.4%	0.9	4.6%	10.1%	5.1%	0.0%	–	44.0%	6.1%	0.3%	237%
vortex	184	0.4%	42%	46.4%	6.9%	3.2	17.6%	0.9%	6.1%	0.7%	36%	14.8%	2.3%	16.2%	1.6%
vpr	6	1.1%	740%	58.1%	16.6%	3.0	162%	0.4%	621%	0.0%	–	16.6%	0.2%	13.8%	2.6%
wave	138	0.9%	55%	60.5%	2.8%	2.4	9.1%	7.3%	1.1%	0.0%	–	40.1%	5.5%	7.7%	2.3%

FIG. 13

Instruction Cache	8k 2-way set-associative, 32 byte blocks, 1 cycle latency
Data Cache	16k 4-way set-associative, 32 byte blocks, 2 cycle latency
Unified L2 Cache	1Meg 4-way set-associative, 32 byte blocks, 20 cycle latency
Memory	150 cycle round trip access
Branch Predictor	hybrid - 8-bit gshare w/ 8k 2-bit predictors + a 8k bimodal predictor
Out-of-Order Issue	out-of-order issue of up to 8 operations per cycle, 128 entry re-order buffer
Mechanism	load/store queue, loads may execute when all prior store addresses are known
Architecture Registers	32 integer, 32 floating point
Functional Units	8-integer ALU, 4-load/store units, 2-FP adders, 2-integer MULT/DIV, 2-FP MULT/DIV
Virtual Memory	8K byte pages, 30 cycle fixed TLB miss latency after earlier-issued instructions complete

FIG. 14

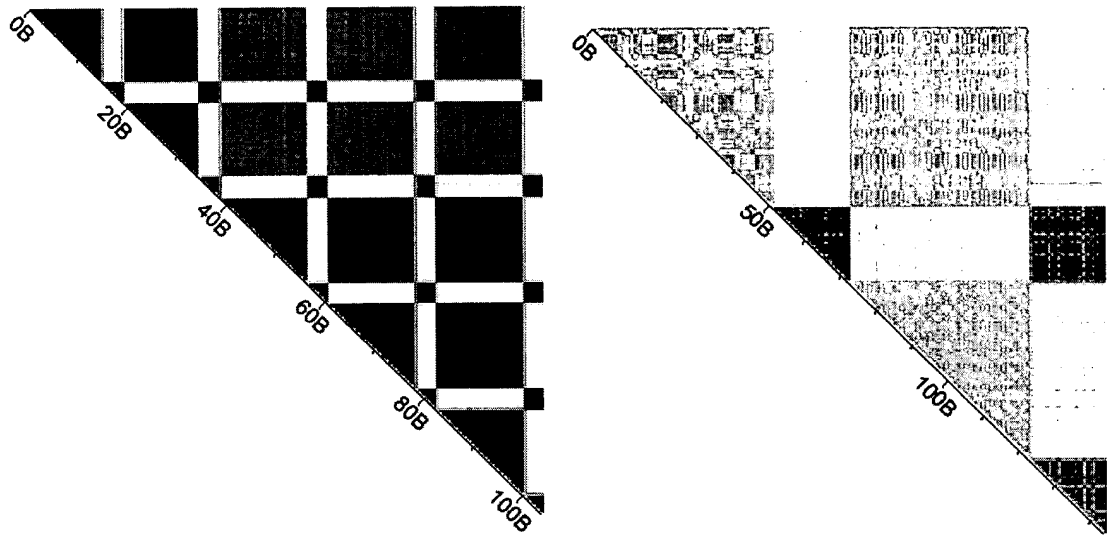

FIG. 15

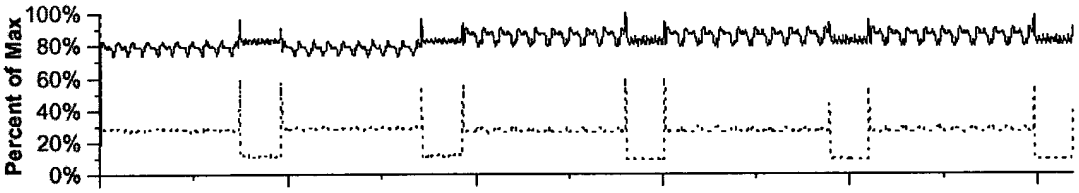

FIG. 16

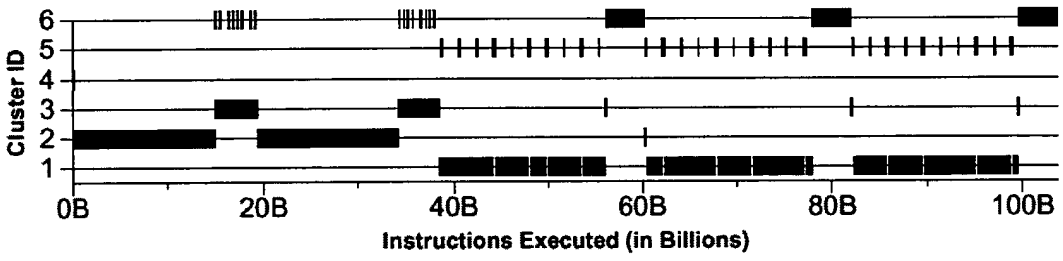

FIG. 17

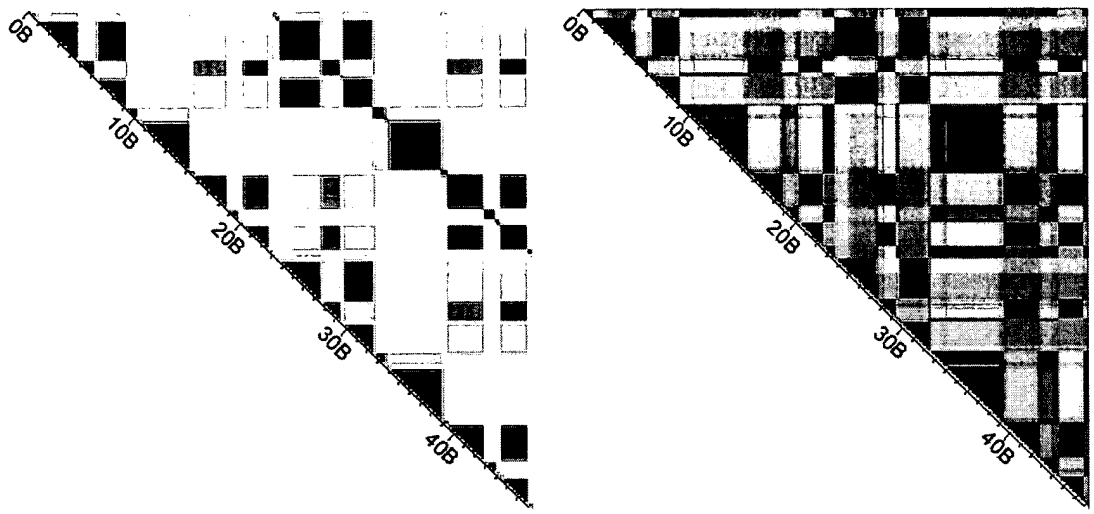

FIG. 18

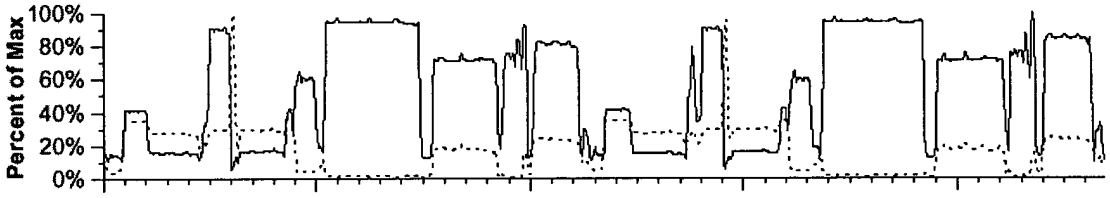

FIG. 19

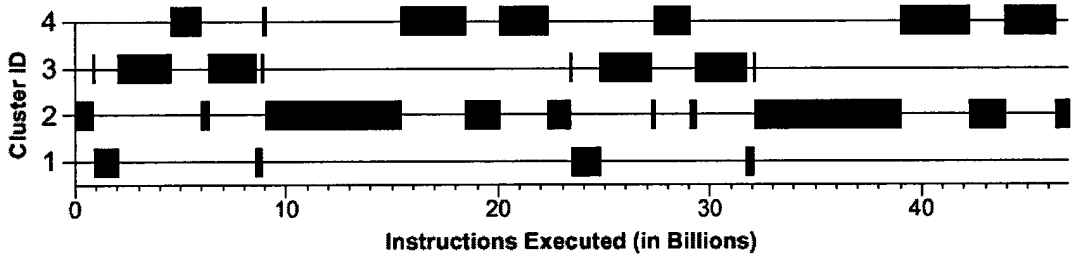

FIG. 20

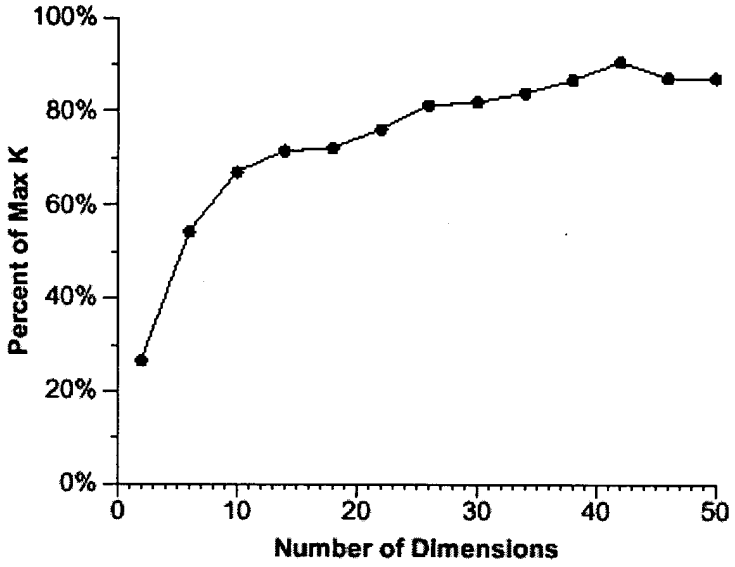
100%
80%
60%
40%
20%
0%
Percent of Max K
0
10
20
30
40
50
Number of Dimensions

FIG. 21

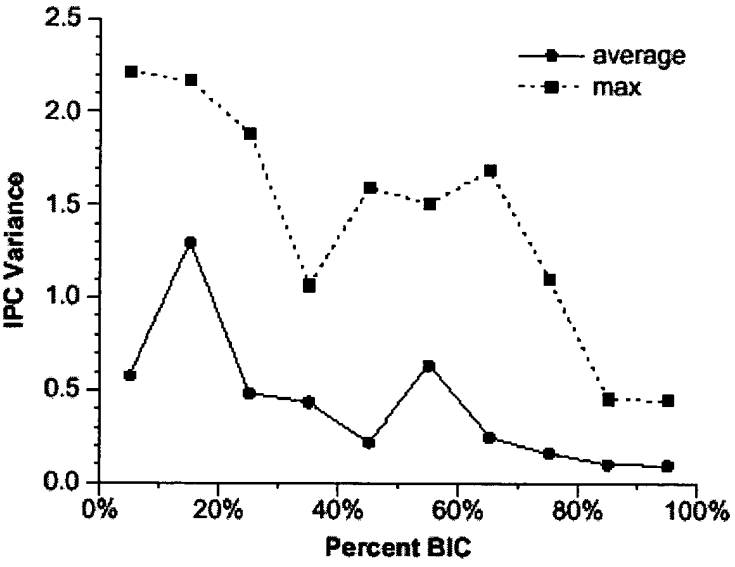
2.5
2.0
1.5
1.0
0.5
0.0
IPC Variance
average
max
0%
20%
40%
60%
80%
100%
Percent BIC

FIG. 22

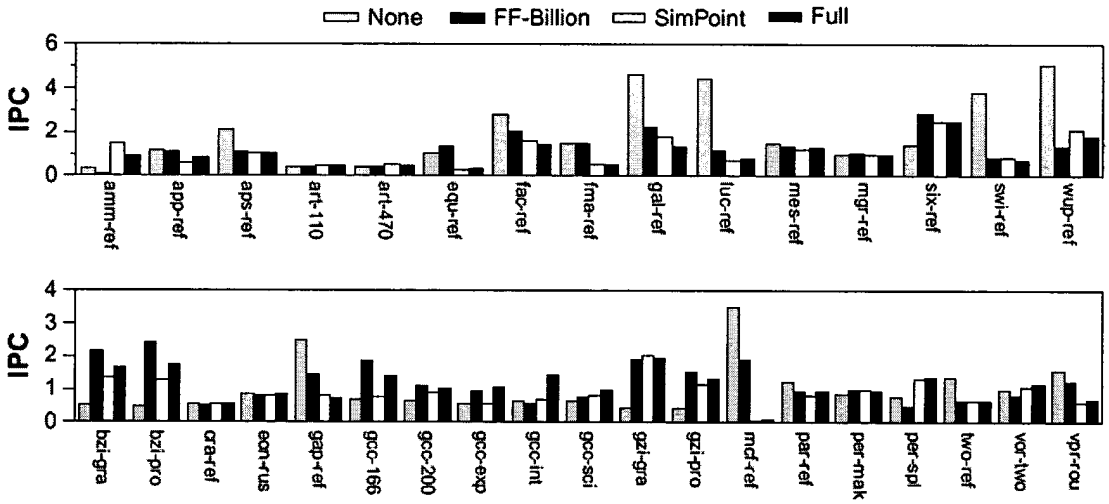

FIG. 23A

FIG. 23B

name	Len	Init	SP	PC	Proc Name	Multiple SimPoints				
ammp	3265	24	109	026834	mm_fv_update.	3026(13.8) 1607(12.6)	1774(31) 2437(4.9)	595(15.3) 3112(11.5)	1068(1.3) 2480(2.2)	2128(7.4)
applu	2238	3	2180	018520	buts_	624(22.1) 1507(14.5)	1625(22.5)	1956(18.8)	2234(6.6)	1390(15.5)
apsi	3479	3	3409	0380ac	dctdxf_	2107(5.6)	2863(14)	1007(70.7)	896(7.7)	1618(2)
art-110	417	75	341	00fbb0	match	82(42.9)	255(41.2)	50(15.8)		
art-470	450	83	366	00f5d0	match	300(36.2)	46(14.7)	236(49.1)		
bzip2-graphic	1435	4	719	012a5c	spec_putc	168(11.7) 519(11.6)	1042(3.7) 872(8.2)	430(7.5) 195(5.6)	762(16.2) 148(2)	106(15.3) 1435(18.2)
bzip2-program	1249	4	459	00ddd0	sortIt	140(11) 1005(7)	468(12.3) 94(6.9)	78(6.2) 606(14)	990(16) 859(14.6)	445(7.4) 341(4.7)
bzip2-source	1088	4	978	00d774	qSort3	395(16) 177(34.7)	511(4.3)	64(29.1)	488(7.3)	530(8.6)
crafty	1918	462	775	021730	SwapXray	123(25)	510(19.7)	664(22.7)	1123(32.5)	
eon-rushmeier	578	140	404	04e1b4	viewingHit	260(6.6)	238(23.7)	337(20.9)	435(35.6)	216(13.1)
equake	1315	35	813	012410	phi0	874(12.2) 62(11.6)	1292(36.7)	463(12.2)	336(24.1)	3(3.2)
facerec	2682	356	376	02d1f4	graphroutines_lo.	1976(60.1)	1528(2.5)	1935(3.9)	1398(29.2)	348(4.3)
fma3d	2683	192	2542	0e3140	scatter_element.	112(7) 509(13)	209(0.6)	842(68.4)	1600(11)	47(0.1)
galgel	4093	3	2492	02db00	syshtn_	3511(5.5) 2181(29)	2081(11) 2161(3.3)	3466(11.2) 1017(5.5)	516(31.6)	2141(2.7)
gap	2695	639	675	050750	CollectGarb	1114(8.2)	1196(58.1)	88(12.7)	2189(14)	2609(7.1)
gcc-166	469	61	390	0d157c	gen_rtx	238(6.4)	149(42.2)	30(21.3)	404(30.1)	
gcc-200	1086	151	737	0ceb04	refers_to_regno.	8(45.8)	587(17.9)	921(10.9)	575(14.5)	1011(11)
gcc-expr	120	27	37	191fd0	validate_change	63(12.5) 88(5)	81(15.8)	42(16.7)	25(4.2)	9(45.8)
gcc-integrate	131	14	5	1198e0	find_single_use.	118(9.2) 73(17.6)	41(27.5)	102(21.4)	9(20.6)	57(3.8)
gcc-scilab	620	139	208	100d54	insert	255(54.2)	39(9.5)	231(13.2)	379(15.8)	170(7.3)
gzip-graphic	1037	158	654	009c00	fill_window	961(45.4) 566(13.4)	87(28.5)	373(7.3)	1(0.1)	461(5.2)
gzip-log	395	91	266	00d280	inflate_codes	207(24.1)	171(16.5)	157(16.7)	330(23.5)	71(19.2)
gzip-program	1688	112	1190	009660	longest_match	228(22.7)	779(21.4)	472(9.1)	1410(20.4)	594(26.4)
gzip-random	821	152	624	00a14c	deflate	484(0.9) 1(0.1)	625(0.2)	580(51)	811(16.8)	200(30.9)
gzip-source	843	68	335	00a224	deflate	248(14.5) 720(2.5)	327(13.2)	167(17.7)	656(27.8)	373(24.4)
lucas	1423	11	546	021ef0	fft_square_	982(21.4)	602(10.7)	1370(21.4)	458(28)	524(18.6)
mcf	618	15	554	00911c	price_out_impl k	268(39.6) 143(3.9)	425(11)	205(30.1)	468(4.5)	316(10.8)
mesa	2816	6	1136	0a30f0	general_textured.	1846(35.3)	2806(0.7)	398(35.3)	977(28.8)	
mgrid	4191	21	3293	016080	resid_	43(24.2)	3459(22.8)	807(20.1)	3110(16.3)	2476(16.6)
parser	5467	388	1147	01edfc	region_valid	3342(25.1)	1771(29.8)	5102(19.7)	2008(19.4)	4772(6)
perlbmk-diff	399	56	142	07f074	regmatch	6(1) 239(31.8)	355(62.7)	11(0.5)	397(0.8)	12(3.3)
perlbmk-make	20	3	12	08268c	Perl_runops_st.	1(5)	20(20)	6(75)		
perlbmk-perf	290	69	6	08268c	Perl_runops_st.	39(59.3)	207(40.7)			
perlbmk-split	1108	162	451	07fc98	regmatch	704(44.9)	596(9.1)	232(21.7)	461(21.8)	501(2.6)
sixtrack	4709	250	3044	167894	thin6d_	6(1.7)	1719(98.3)			
swim	2258	3	2080	019130	calc1_	1951(29.8)	38(14)	777(24.7)	710(13.8)	2101(17.8)
twolf	3464	7	1067	041094	ucxx1	312(17)	2888(11.3)	3268(11.7)	961(20.4)	2054(39.5)
vortex-one	1189	36	272	06289c	Mem_GetWord	536(17.1)	366(23.3)	115(8.2)	1068(17.2)	878(34.2)
vortex-three	1330	177	565	0336a8	Part_Delete	934(25.4) 485(25.4)	1129(11.4)	96(8.9)	47(11.1)	586(17.8)
vortex-two	1386	206	1025	05e6fc	Mem_NewRegion	635(7.6) 397(23.2)	752(24.5)	554(21.9)	930(7.4)	360(15.3)
vpr-place	1122	4	593	0224ec	get_non_update.	166(25.5) 547(27.9)	857(21.6)	1(0.2)	362(12.8)	1057(12)
vpr-route	840	12	477	025c80	get_heap_head	559(29.9)	89(28)	353(23.8)	3(2.6)	490(15.7)
wupwise	3496	11	3238	01d680	zgemm_	1811(43.3)	91(8)	3055(43.2)	1524(5.4)	

FIG. 24

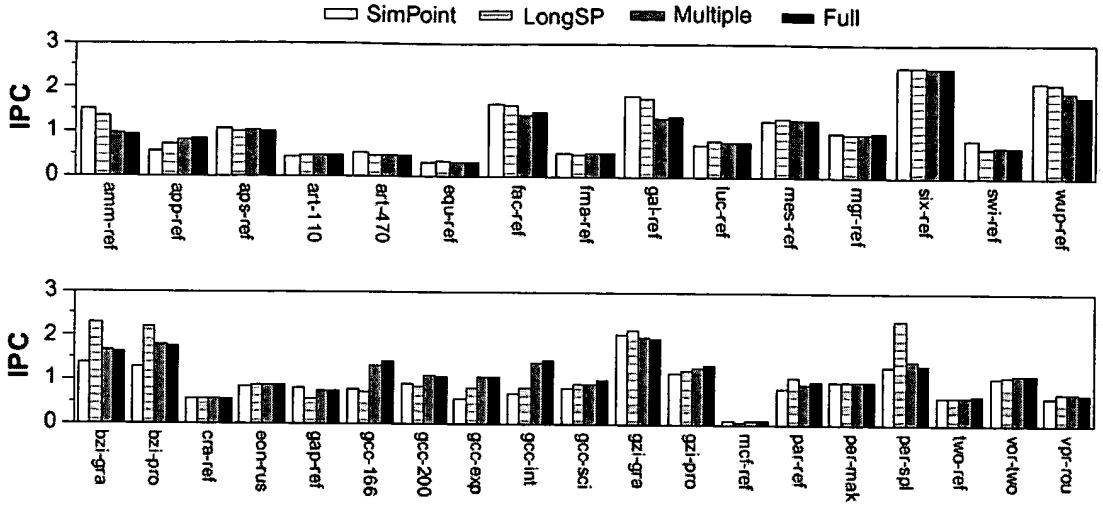

FIG. 25A

FIG. 25B

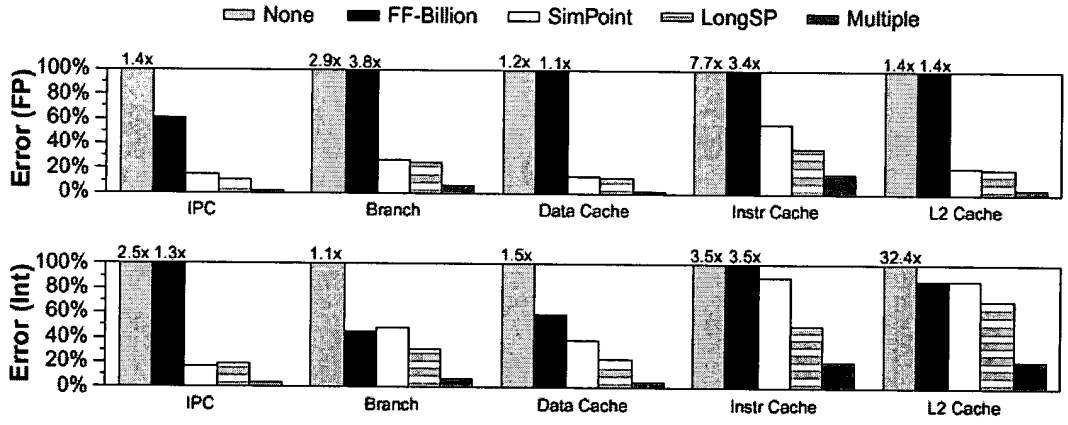

FIG. 26A

FIG. 26B

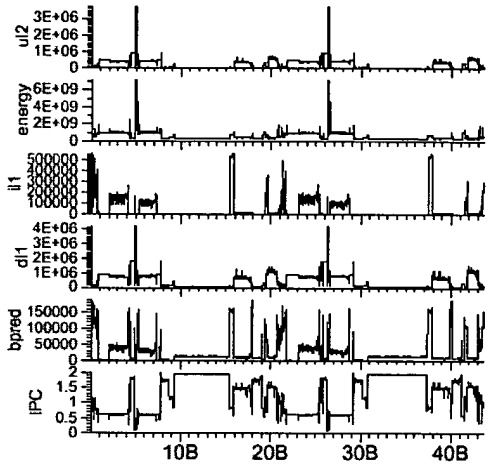

FIG. 27A

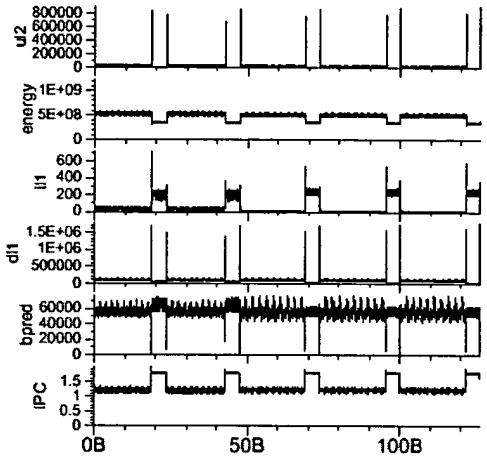

FIG. 27B

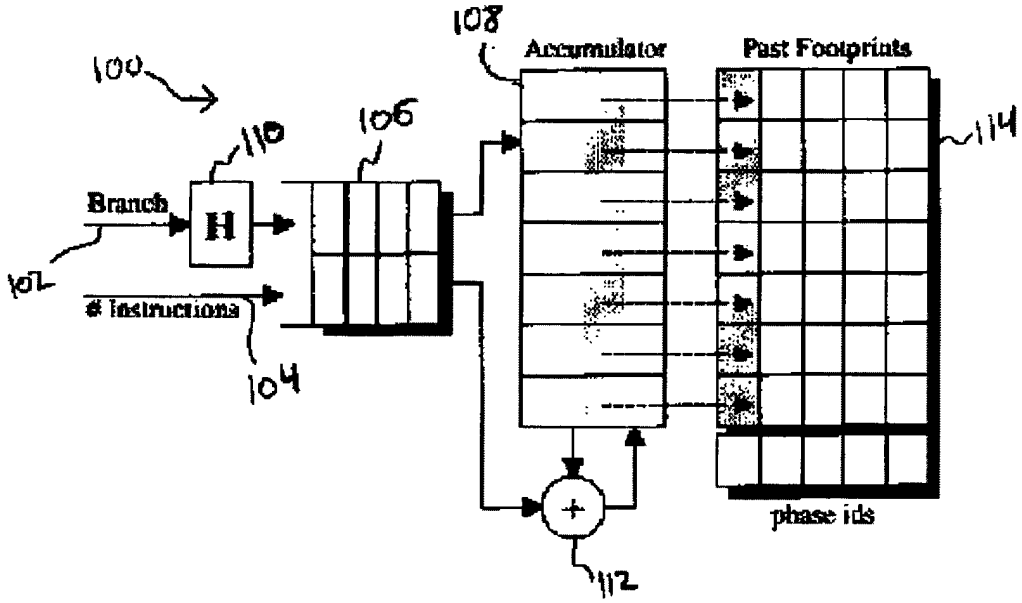

FIG. 28

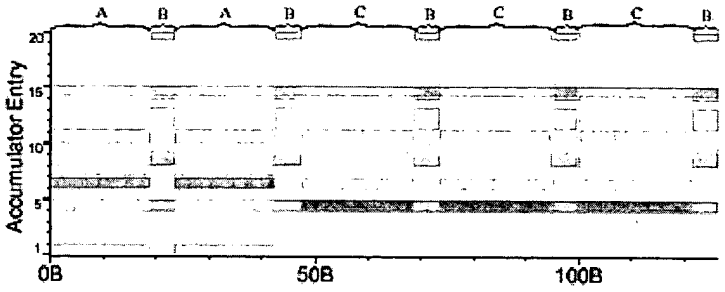

FIG. 29

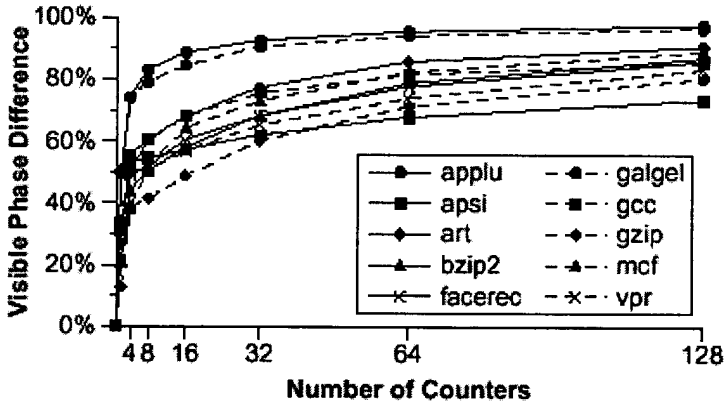

FIG. 30

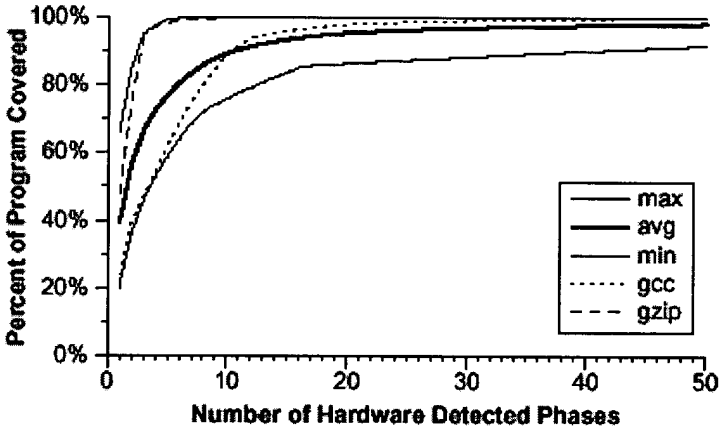

FIG. 31

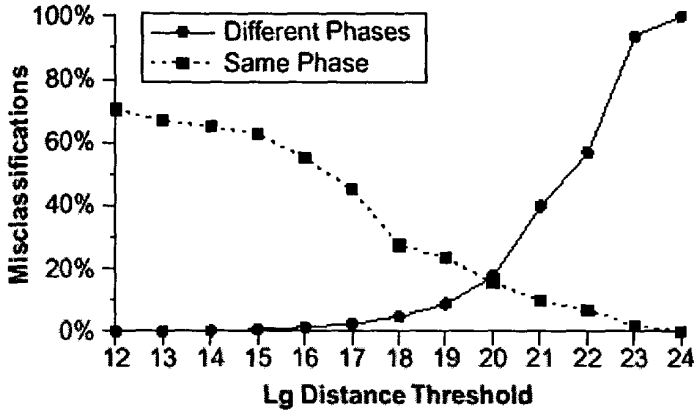

FIG. 32

	phase	IPC	(stddev)	bpred	(stddev)	dl1	(stddev)	il1	(stddev)	energy	(stddev)	ul2	(stddev)
gcc	full	1.32	(43.4%)	27741	(135.5%)	445083	(110.7%)	50763	(203.2%)	6.44E+08	(90.0%)	227912	(139.7%)
	18.5%	0.61	(1.6%)	34665	(22.0%)	753382	(5.4%)	125091	(23.2%)	1.03E+09	(1.8%)	395997	(5.3%)
	18.1%	1.95	(0.3%)	13048	(3.9%)	28112	(15.1%)	43	(73.9%)	3.22E+08	(0.2%)	1006	(5.6%)
	7.2%	0.64	(0.2%)	843	(15.1%)	885081	(0.1%)	75	(215.5%)	9.78E+08	(0.3%)	443655	(0.1%)
	4.0%	1.49	(1.2%)	10145	(7.6%)	703554	(6.8%)	15591	(5.2%)	4.20E+08	(1.1%)	354084	(7.0%)
	3.9%	1.76	(1.6%)	2015	(13.6%)	98947	(5.9%)	102	(45.1%)	3.57E+08	(1.6%)	15595	(12.6%)
	phase	IPC	(stddev)	bpred	(stddev)	dl1	(stddev)	il1	(stddev)	energy	(stddev)	ul2	(stddev)
gzip	full	1.33	(16.3%)	56045	(11.1%)	90446	(58.2%)	60	(138.1%)	4.82E+08	(13.5%)	22880	(112.0%)
	17.1%	1.24	(3.4%)	53300	(10.8%)	96960	(10.1%)	12	(44.2%)	5.05E+08	(3.5%)	24218	(8.6%)
	9.4%	1.23	(3.8%)	54973	(11.5%)	99523	(11.3%)	11	(45.5%)	5.09E+08	(3.8%)	24518	(9.3%)
	8.8%	1.76	(0.6%)	56449	(4.8%)	37331	(5.6%)	241	(8.4%)	3.55E+08	(0.6%)	5617	(15.6%)
	8.0%	1.22	(4.3%)	54791	(6.8%)	99671	(11.9%)	40	(25.7%)	5.14E+08	(4.4%)	28153	(11.0%)
	7.4%	1.24	(3.1%)	55215	(11.1%)	96701	(9.6%)	12	(35.4%)	5.04E+08	(3.2%)	23701	(8.4%)

FIG. 33

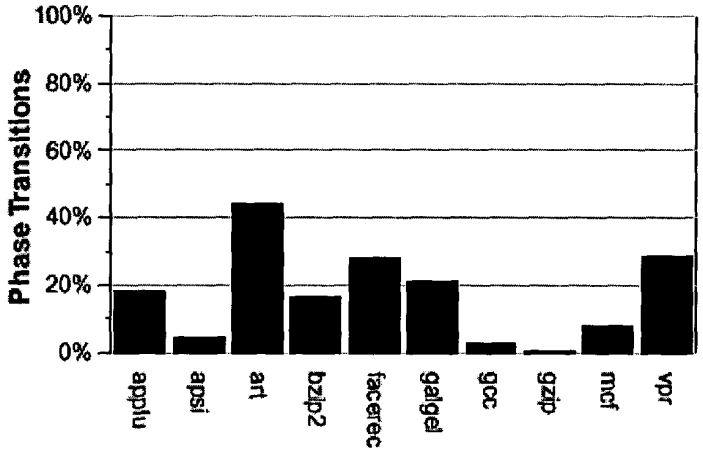

FIG. 34

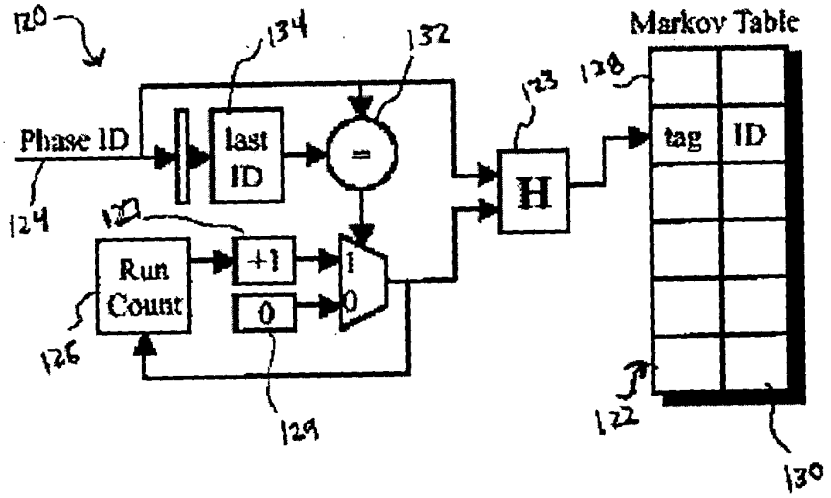
120
134
132
Markov Table
128
123
Phase ID
last ID
-
H
tag
ID
124
121
Run Count
+1
0
1
0
126
129
122
130

FIG. 35

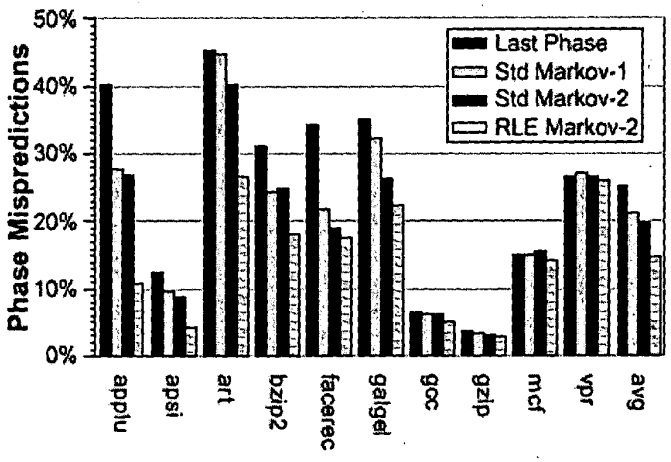
50%
40%
30%
20%
10%
0%
Phase Mispredictions
Last Phase
Std Markov-1
Std Markov-2
RLE Markov-2
applu
apsi
art
bzip2
facerec
galgel
gcc
gzip
mcf
vpr
avg

FIG. 36